

MUHAMMAD AFFAN NUR IMAN BIN AZMAN

CUSTOM IC LAYOUT ENGINEER

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Professional Summary

Custom Layout Engineer Trainee with Cadence Virtuoso experience in 40 nm CMOS standard cells and TSMC 28 nm analog layout. Completed DRC-clean and LVS-matched bandgap-reference and operational-amplifier layouts through schematic interpretation, floorplanning, matched-device placement, manual routing and verification debugging. Mechatronics Engineering graduate with supporting experience in Python, embedded systems and multidisciplinary hardware integration.

Custom IC Layout Experience

Custom Layout Engineer Trainee | Vchip Technology, Penang | Jun 2026 - Present

On-the-job training scheduled through 31 October 2026; early release may be arranged with Vchip upon receipt of a formal offer letter.

- Developed 40 nm CMOS standard-cell layouts in Cadence Virtuoso using the CMOS040 RunPeng PDK, including single- and multi-finger inverters, NAND, NOR, AND, OR, XOR, NAND3, NOR3, half adders and full adders.
- Completed TSMC 28 nm operational-amplifier and bandgap-reference layout iterations with DRC-clean and LVS-matched results.
- Applied schematic interpretation, analog floorplanning, device matching, symmetry, diffusion sharing, manual routing and supply planning across MOS, BJT, resistor and capacitor networks.
- Refined device placement and routing after engineering reviews, including feedback on BJT proximity and critical-device symmetry.
- Resolved geometry and connectivity violations through iterative DRC/LVS checks and PDK rule interpretation; configured Virtuoso bindkeys and workspace tools to support layout debugging.
- Progressed to top-level floorplanning for a separate bandgap-reference design integrated with an LDO, planning placement and routing around critical signals and supply nets.

Technical Skills

EDA tools: Cadence Virtuoso; Synopsys Custom Compiler and IC Validator (training).

Process nodes and blocks: 40 nm CMOS standard cells; TSMC 28 nm operational amplifier and bandgap reference; LDO top-level floorplanning; SAED32nm academic PDK.

Custom layout: Schematic interpretation, floorplanning, multi-finger devices, diffusion sharing, matched-device placement, symmetry, common-centroid and interdigitated placement, manual routing and power rails.

Physical verification: DRC, LVS, connectivity and geometry debugging, and PDK design-rule interpretation.

Circuit and layout knowledge: Differential pairs, current mirrors, BJT cores, resistor networks and capacitors; working knowledge of WPE, LOD, OSE/PSE, guard rings, well and substrate taps, latch-up, antenna effects and parasitic RC.

Programming and systems: Python, C/C++, Linux; introductory Cadence SKILL; ROS, embedded controllers and sensor integration.

Education

Bachelor's Degree in Mechatronics Engineering - Second Class Upper

Universiti Sains Malaysia | Nibong Tebal, Penang | Nov 2025

Certifications and Technical Training

Cadence | Sep 2026

Virtuoso Layout Design Basics v1C25.1 Exam; Semiconductor 101 v3.0 Exam.

IC Design Custom Layout | Penang Skills Development Centre | May - Jun 2026

Completed SAED32nm digital custom-layout exercises in Synopsys Custom Compiler and IC Validator, covering logic gates including NAND and XOR, SRAM, half adder, full adder, hierarchical 8-bit and 16-bit full adders, and DRC/LVS verification practice.

Chip Start 2.0 | ASEM | Mar 2026

Participated in introductory digital and analog IC design training.

Custom Layout One-Day Bootcamp | ASEM and SkyeChip | Feb 2026

Completed an SAED32nm inverter layout with dummy devices and achieved a clean DRC result using Synopsys IC Validator.

Additional training: CMOS Analog Circuit Design, Udemy (May 2026); Introduction to Semiconductor Manufacturing, Udemy (Jun 2026); Arm On-Demand Training, Arm (Oct 2025); FPGA and AI Training, USM and Lattice Semiconductor (Apr 2025).

Additional Engineering Experience

Research Assistant - Autonomous UAV | Universiti Sains Malaysia | Feb 2025 - Jun 2026

Part-time research and development

- Developed Pixhawk-based UAV platforms and control software using ArduPilot/PX4; integrated Raspberry Pi 5 companion computing and telemetry.
- Tested flight commands and navigation behaviour using PX4 SITL in Gazebo.

Research Assistant - Unmanned Surface Vehicle | Universiti Sains Malaysia | Aug 2025 - Jan 2026

PETRONAS Research project | Contract

- Restored a Clearpath Heron M300 after computer and SSD failure, troubleshooting ROS, propulsion, networking and navigation sensors.
- Supported ROS/Gazebo integration, PID tuning and pool testing of a gyrostabilisation prototype.

Robotic Engineer Trainee | Cytron Technologies Sdn Bhd | Jul 2024 - Oct 2024

Internship

- Developed a Micro:bit line-following and pick-and-place robot using IR sensing and HuskyLens vision; contributed to microdrone STEM-kit research.
- Produced 15 product tutorials and led a Raspberry Pi AI-vision workshop at Politeknik Seberang Perai.

Selected Engineering Project

Twin Gyrostabilizer for an Unmanned Surface Vehicle | Nov 2024 - Jul 2025

Final-year project | Universiti Sains Malaysia | PETRONAS Research project

- Designed and tested a twin-flywheel stabilisation system using BLDC motors, servo actuation, PID control and IMU-based state estimation.
- Bench and pool tests reduced maximum roll from approximately 35 degrees to 10 degrees and settling time from 15.85 s to 4.10 s under the tested conditions.

Leadership and Languages

Cadet Officer, USM ROTU Army (2022 - 2024); Technical Team Committee, USM Drone Club (2023 - 2024).

Malay - native | English - professional working proficiency